The Gilbert Cell

Henry Jung
Department of Electrical and Computer Engineering
Rose-Hulman Institute of Technology
Terre Haute, Indiana, U.S
jungh@rose-hulman.edu

Tina Hudson Simoni
Department of Electrical and Computer Engineering
Rose-Hulman Institute of Technology
Terre Haute, Indiana, U.S
hudson@rose-hulman.edu

***Abstract* — A variety of analog integrated circuits (ICs) contain operational amplifiers, which consist of two transistors forming a differential pair. There are many types of differential pairs used today. The two important aspects in a differential pair: Its gain is determined by a function of the tail current, otherwise known as the bias network, and two transistors in a pair that can steer the bias network into one of the transistors. [1] In this paper, these aspects of differential pairs are taken to the next level to understand the design and implementation of an existing type of variable-gain amplifier (VGA).**

I. Introduction

It was February 2026 when Dr. Tina Hudson, professor of Electrical and Computer Engineering at Rose-Hulman Institute of Technology, proposed an idea to a certain student for an independent study/research opportunity for the Analog IC design course elective. Because a certain student missed the enrollment window for the elective in September 2025 due to limited circumstances, Dr. Hudson kindly decided to allocate some of their time to offer the student an amazing opportunity before their graduation. The student's responsibility was to self-guide through the lecture notes and laboratory assignments to build the necessary IC design skills to implement a Variable Gain Amplifier. With this objective, the independent study course was named "IC Design of A Variable Gain Amplifier."

II. Gilbert Cell Overview

If this differential pair were to have variable gain and control via an external voltage, it would be called a variable-gain amplifier (VGA). As seen in Figure 1, the Gilbert Cell is another type of VGA whose gain can range from negative to positive values. It is composed of two differential pairs (4 total transistors, M1 – M4), with their outputs nested in an alternating pattern, and two external voltages that define the currents through each differential pair. These voltages, responsible for steering the current I_{SS} between two pairs in opposite directions, are called the control voltages ($V_{cont1,}V_{cont2}$). If there is a circuit that can vary the direction of the current via voltages, that would be another differential pair with voltage inputs. Thus, M5 and M6 are added to meet the need. M1 – M4 are matched, and M5 and M6 are matched. R_D can either be replaced with an active load or a diode-connected transistor.

III. Methodology

The overall implementation process for a Gilbert Cell will be introduced, from initial design calculations for the desired specifications to simulation and adjustment, through layout and extraction. All steps were guided using the Skywater 130nm process (SKY130) design rules [2], and all circuit simulations and implementations were performed using Cadence Virtuoso software. [3]

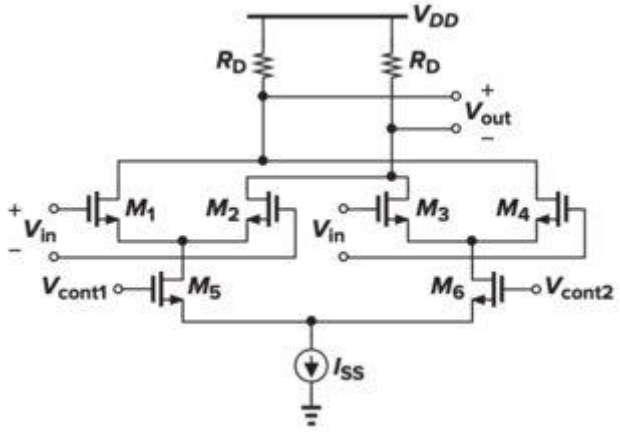

Fig. 1. The Gilbert Cell

IV. Initial Calculations

The first step was to determine the channel width-to-length ratio (W/L) for each device to meet the desired theoretical specification. This was a simple algebraic process using the known parameters from early laboratory assignments characterizing N-type and P-type field-effect transistors (n-FET and p-FET) for SKY130, 10V power supply rails (V_{DD}), along with general equations for gain (2) and DC current (I_{DQ}) (1). I_{SS} is the current bias network already designed from previous laboratory assignments, outputting 730uA. Using KCL, I_{DQ} through the active loads, M5, and M6 are halved (365uA), and halved again for M1 – M4 (182.5 uA). The desired specification included the allowable swing of 2.5V and an AC gain magnitude of ±25. Summary of known parameters from characterization is shown in Table 1. The naming convention can continuously vary based on what FET type is being used for analysis, i.e., p-type uses μCox_p and $V_{SG,}V_{SD}$ conventions while n-type uses μCox_n and $V_{GS,}V_{DS}$.

$$I_{DQ} = \frac{1}{2} * \mu Cox_p * \frac{W}{L}(V_{SG} - V_T)^2(1 + \lambda * V_{SD}) \quad (1)$$

$$Av = \sqrt{2 * \mu Cox_n \frac{W}{L} I_{DQ}} * (R_{op}||R_{on}) \quad (2)$$

$$R_o = \frac{1}{\lambda * I_{DQ}} \quad (3)$$

TABLE I.

FET Type	$\mu Cox(10^{-6})$	λ	$V_T(V)$
N-FET	64.6	0.05	0.75
P-FET	36	0.02	1.2

p-FET active loads were chosen as an alternative option for R_D, due to its higher output resistance R_{OP} compared to diode-connected loads. Since active loads require a consistent gate voltage to operate, a separate bias network is required to supply this DC voltage. This voltage is called V_B. This meant that V_B also sets the source-gate voltage V_{SG} because $V_S = V_{DD}$. With the desired swing of 2.5V and accounting for an additional 1V upper headroom, the starting Q-point was set as 6.5V, which set the target V_{SD} to be 6.5V. Using (1) and an arbitrary target V_{SG} At 3.5V for the active loads, the W/L was estimated at around 4.

The circuit for generating V_B was also designed using a similar process. It consisted of two diode-connected p-FETs with V_{SG} of 3.5V cascoded on top of n-FET with the intent to drop a total of 7V from the V_{DD} rail, allowing n-FET with the V_{GS} of 3V, shown in Figure 2. $V_{SD} = V_{SG}$ for diode-connected FETs, which allowed the use of (1). using (2) and (3), the W/L ratio for the signal FETs (M1 – M4) was calculated to be around 10. Calculations for W/L of M5 and M6 used (1) involved a different process. An independent differential amplifier was first designed using I_{SS}. The calculated W/L for n-FET was 12, and the bottom half of the amplifier was used as M5 and M6.

All devices used a unified channel length of 2 µm. With the initially determined W/L ratios, the width of active load p-FETs, M1 – M4, and M5 & M6 were 8 µm, 20 µm, and 24 µm, respectively.

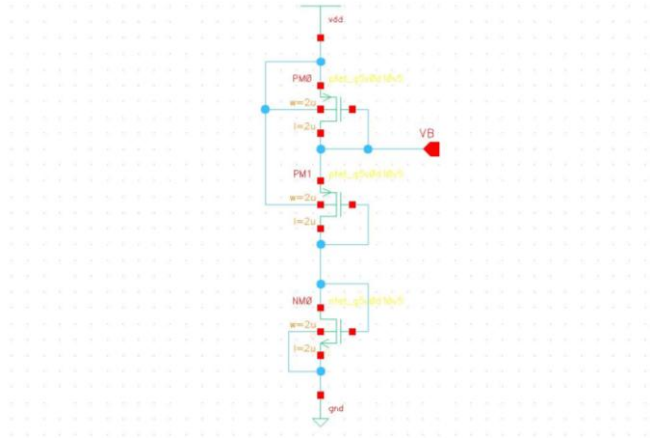

Fig. 2. DC Voltage Network

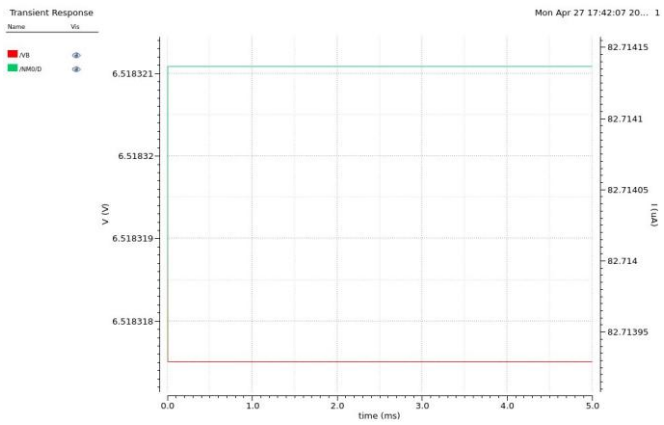

Fig. 3. Transient Analysis of VB

V. Initial Simulations and Issues with VB

A transient response of V_B for the active load was recorded. The network was designed to output around 6.5V to achieve the V_{SG} of 3.5V for the (p-FET) for the Gilbert Cell. Now, the task was to find the common-mode input range for the control voltage (V_{CM_cont}), then input voltage (V_{CM_in}).

To find V_{CM_cont}, the input voltage (the gate voltage for M1–M4) was set to a high value but below V_{DD} (10V). This was set to be 8V. This way, the source voltages of M1–M4 are not close to the low point where they could push M5 and M6 out of the saturation region. It was found that the output voltage (V_{out}) (net 3) remains relatively constant when V_{cont} is greater than 2.5V, as shown in Fig. 4.

The first issue encountered was that the voltage at the common-source node of the control-voltage FETs (M5–M6) was too low, causing the I_{SS} (I bias) FET to operate below the saturation region. The intended 750uA bias network was broken, outputting only slightly above 600uA, as shown by Iout in Fig 4.

In addition to I-bias, the DC bias point for both outputs was much lower than the intended 6V. To diagnose the problem more deeply, a parameterized sweep (nested sweep) was performed using DC analysis over the input voltage range from 0.1 to 10 V, with the control voltage (V_{cont}) as a parameter. The V_{out} is plotted in Figure 5.

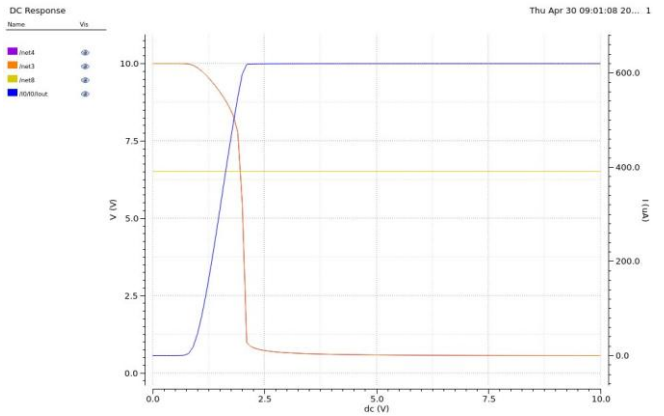

Fig. 4. DC analysis of Vcont from 0 to 10V

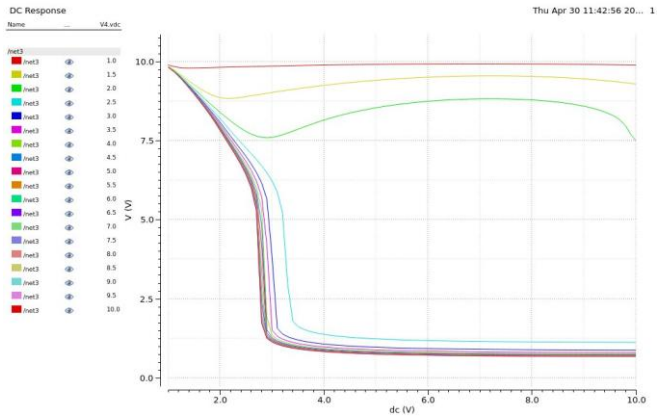

Fig. 5. Vout with DC analysis of Vin from 0 to 10V w/ paramterized sweep of Vcont, VB = 6.5V

For V_{cont} ranging from 2.5V to 10V, Vout was constant, with its DC bias point much lower. However, this result matched the discovery from the previous simulation, where the output remained relatively constant after V_{cont} exceeded 2.5V. To address this problem, the bias voltage of the active load was varied and simulated. First, the V_B network was modified by adding an additional p-FET network, thereby decreasing the overall V_{SG} in each p-FET and increasing V_B to achieve a lower source-drain saturation voltage($V_{SD,SAT}$) for the active load.

$$V_{DS,SAT} = V_{SG} - |V_T| \tag{4}$$

VI. Simulation with Multiple VB

The initial setting for the V_{SG} was around 2.2V to allow the $V_{SD,SAT}$ of the active load to be 1V, with $|V_T|$ around 1.2V from the Skywater 130nm characterization process. To achieve this, the VB network was set to output around 7.78V, with W/L adjusted using (1). The bias network output current reached the desired value of 730uA for any V_{cont} above 3.0 V, as shown in Figure 6. The behavior of V_{out} was still under investigation, as more information was needed from different settings. Through this adjustment, it was determined that I_{SS} was not operating in the saturation region when the V_{SG} of the active load was 3.5 V.

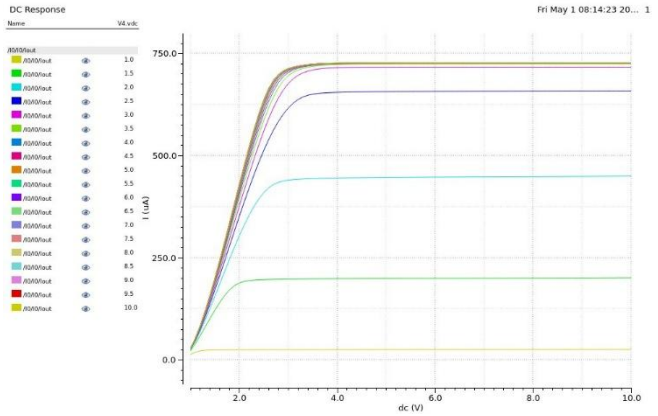

Fig. 6. Iout (Bias Network) with DC analysis of Vin from 0 to 10V, with varying Vcont from 1V to 10V, VB = 7.78V

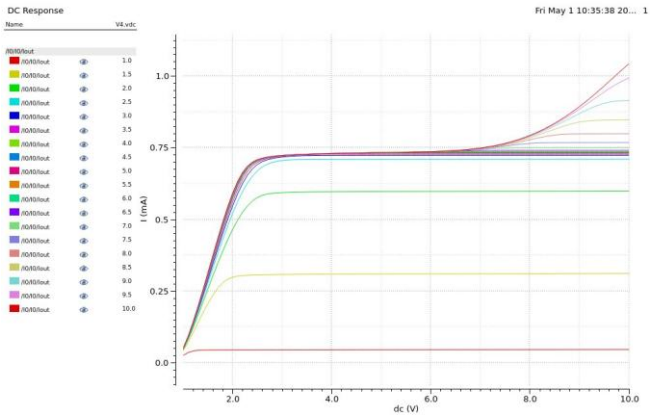

Fig. 7. I-bias (Bias Network) with DC analysis of Vin from 0 to 10V, with varying Vcont from 1V to 10V, VB = 7.97V

As the $V_{SD,SAT}$ of the active load was now around 1V, which provided more upper headroom for the output swing. In addition, any V_{cont} greater than 3V would allow the bias network to remain within the saturation region without experiencing short-channel effects.

To increase upper headroom, V_B was slightly increased to 7.97V. This would reduce the V_{SG} of the active load to 2.08V and the $V_{SD,SAT}$ to around 0.8V. Increased upper headroom indicated a greater common-mode input range for Vin and a wider operating range for V_{cont}. As V_{cont} increases, the source voltage of M5 and M6 (V_{S5} & V_{S6}), which are the same, also increases. This also meant that V_{S5} & V_{S6} could reach higher voltages than when V_B was 2.22V, which began to introduce short-channel effects in the bias network for the current source after V_{cont} reached a certain level (around 7.5V), as shown in Figure 5.

However, determining the behavior of V_{out} remained to be a task, as it was difficult to understand what was causing the value to fluctuate. Shown in Figure 8, the drop in V_{out} was also observable as short-channel effects were introduced. As short-channel effects increase current through the bias network, they increase the current through the active load, raising its V_{DS} and pushing down V_{out} .

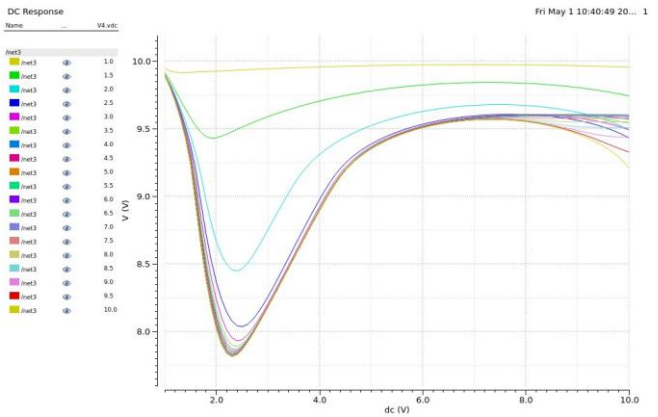

Fig. 8. Vout with DC analysis of Vin from 0 to 10V, with varying Vcont from 1V to 10V, VB = 7.97V

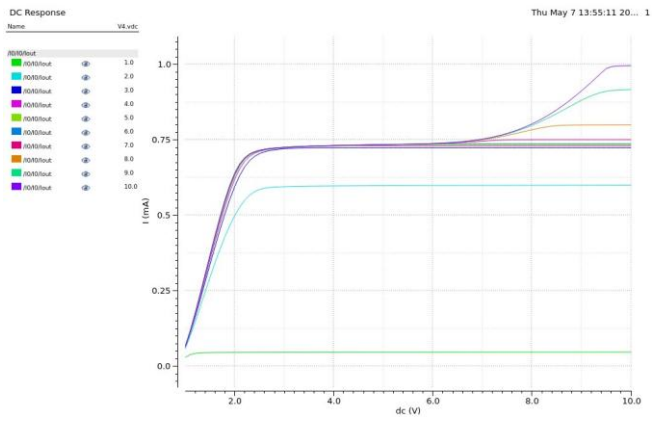

Fig. 9. Vout with DC analysis of Vin from 0 to 10V, with varying Vcont from 1V to 10V, VB = 8.2V

Using (1), the V_B was increased once again to 8.2V, with proper adjustment of W/L. The behavior of the bias network was similar to when V_B was 7.97V. Both plots in Figures 7 and 9 provide a good estimate of the permitted range of V_{cont} around 3V to 7V. This is the range where the bias network is in its saturation region, without introducing short-channel effects.

While the upper headroom for swing was improved by decreasing V_{Sg} for the active load, it came with a compensation of area, as the W/L ratio for the active load FET was reaching near the 50's with V_B = 8.2V, summarized in Table II. These FETs with big W/L can be handled by connecting smaller ones, ones with a smaller width but same length in parallel; the area could go out of control, especially when there are two active loads, not just one. It was also important to consider that reducing the V_{SG} could introduce additional unwanted short-channel effects in the bias network, as V_{S5} & V_{S6} could be increased further.

Again, through a few simulations with different V_B values, it was possible to determine a good V_{cont} range of 3V to 7V, and a good Vin range of 3V to 6.5V. It is crucial, however, to understand that this result is only valid for ensuring proper operation of the bias network, not for all the other FETs in the circuit. A good V_B range, to maximize swing while not causing the FET to be too big, was reasonably determined to be somewhere between 7.8V and 8.2V. But because V_B is not a range but a set value, it would require more simulation data with various environments to find a sweet spot.

VII. Characterization of VDS

One of the main reasons it was uncertain to determine the ranges for various inputs was the back-gate effects. The n-FETs for V_{cont} and V_{in} have tap (bulk) connections tied to ground, while the source connections are at a higher potential than ground due to the voltage drop across the bias network.

TABLE II.

VB	7.78 V	7.97 V	8.2 V
VSG	2.22 V	2.08 V	1.8 V
W/L Ratio	17.88	29.12	52.12

Fig. 10. Summary of the increase of VB with changing W/L of active load pFET.

The n-FETs for V_{in} (M1–M4) were expected to experience a greater back-gate effect due to the additional voltage drop across M5 and M6. Back-gate effects cause higher V_T, which requires either a higher offset for V_{cont} and V_{in} or a greater W/L ratio for all M1 through M6 to satisfy the (4).

Even though the previous simulation accounted for back-gate effects, it was necessary to observe changes in V_{DS} as Vin varied, since it required all FETs to operate in the saturation region for proper functionality of the entire Gilbert Cell at its Q-point and when it is swinging. Thus, to better understand how to choose the Q-point and min/max swing, this step was added. Past simulations suggested that a good V_{cont} range for normal operation of the bias network was between 3V and 7V. V_{cont} was fixed at 3V, and the changes in V_{DS} for (M1 ~ M4) and (M5 & M6) were recorded over a range of V_{in} from 1V to 10V, with different V_B values of 7.78V, 8.2V, and 8.3V, in figures 11, 12, and 13, respectively.

The dashed lines are the estimated $V_{SD,SAT}$ and $V_{DS,SAT}$ for each nFET group and the Active Load, respectively, accounting for the back-gate effect. One positive aspect of the back-gate effect was that it reduced the $V_{DS,SAT}$ by increasing the threshold voltage, thereby providing more headroom for the swing. The goal was to find a range of V_{in} where all V_{DS}, V_{SD}, and bias networks operate above their saturation points.

A. VB = 7.78V

V_B at 7.78V provided $V_{DS,SAT}$ of around 1V, leaving much less headroom than expected. As seen in the figure. 13, the active load gets pushed into the linear region at V_{in} a little above 3V, even before the V_{DS} of M1 – M4 reaches the saturation point. From this simulation, it was concluded that there is no valid range of Vin that guarantees a saturation region for all FETs, and that more upper headroom is needed. Thus, V_B needed an increase.

B. VB = 8.2V

This V_B value yields a V_{SG} of 1.8V and a $V_{DS,SAT}$ of 0.6V using (1). There was a working range of Vin with this setting, as the V_{DS} of the active load remained above the saturation region long enough for the V_{DS} of M5 and M6 to reach the saturation point. Not long after, the active load was pushed into the linear region, which made the allowable range of V_{in} very tight (4V–5V), as shown in Figure 12. There was a solution to work with, but the swing and gain specification would most likely not have met the desired.

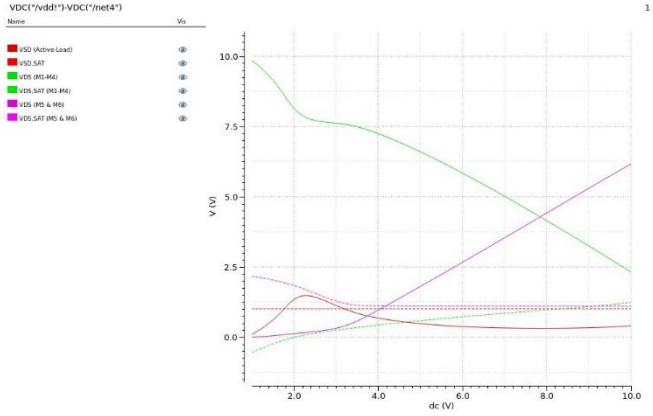

Fig. 11. VDS analysis with changing Vin, VB =7.78

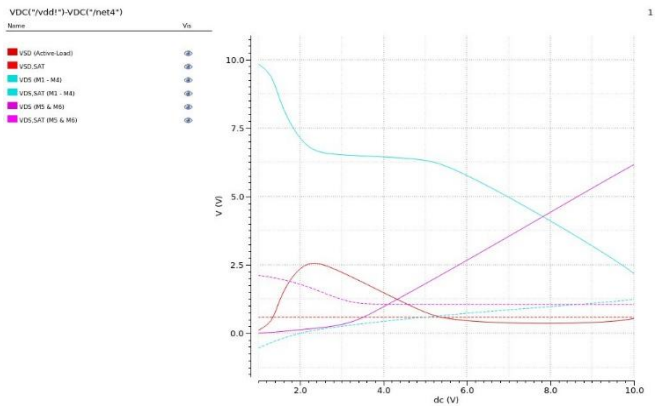

Fig. 12. VDS analysis with changing Vin, VB =8.2

C. *VB = 8.3V*

V_{SG} of the active load was now 1.7V, with $V_{SD,SAT}$ at 0.5V. The V_{SD} now remain above the saturation point for an extended period, providing a much wider V_{in} range to work with, as shown in Figure 13. The plot in Figure 13 shows all FETs operating in a saturation region after V_{in} = 4.2V. However, the upper limit of Vin was reached sooner than for any other FET, as V_{out} reached its max value, coinciding with the active load hovering at the edge of saturation (around V_{in} = 7.5V). This V_B value provided a much wider common-mode input range (CMIR) for Vin, from around 4V to 7.5V. This was also the maximum V_B , i.e, the lowest allowable $V_{SD,SAT}$, as W/L was becoming significantly large. With the allowable V_{in}, the estimated V_{out} range was approximately 7.75V to 9.5V. With this range, it was reasonable to set the Q-point (DC offset) of V_{out} to be 8.6V, which was the middle of the range, for the purpose of maximizing swing. The last step was to re-verify that the bias network is functioning properly. As shown in Figure 14, it operated in the consistent saturation region (730 µA) within the allowable V_{in} range found.

The final width of the active load was adjusted to just under 100 µ meters (96 µ meters), yielding a W/L ratio of around 48. To allow the 8.3V DC output on the voltage bias network, an additional p-FET was added on the cascode, and only the top p-FET's width was adjusted to 9 µm (W/L = 4.5).

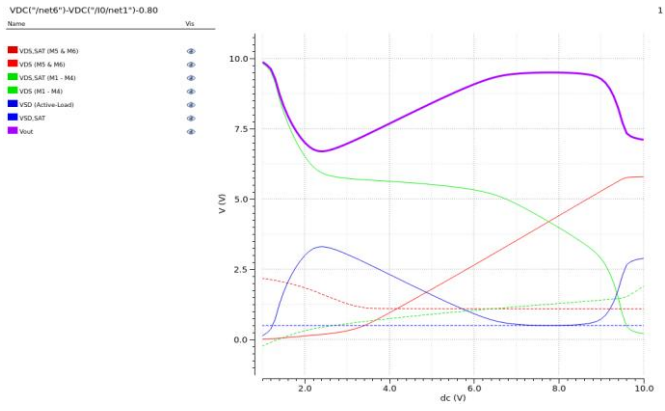

Fig. 13. VDS analysis with changing Vin, VB =8.3

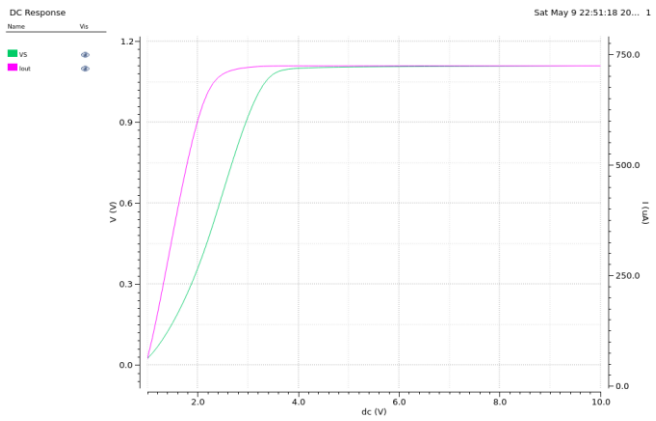

Fig. 14. Iout and VS5 & VS6 at VB =8.3

VIII. Control Voltage Range and Body Effects

The Q-point for Vout was set around 8.6V. From the plot in Figure 13, the input voltage was about 5.2V when Vout was 8.6V. Thus, the common-mode input voltage (V_{CM_in}) as 5.2V. Gilbert Cell is a cascode structure, differential pairs (M1 – M4) stacked on top of another differential pair (M5 & M6), that consumes greater headroom for output swing. To ensure M5 and M6 operate in the saturation region, the common mode of the control voltage (V_{CM_Cont}) must stay at a certain level under V_{CM_in}. Assuming M1 – M4 are matched and M5 & M6 are matched, the calculations for maximum V_{CM_Cont} becomes:

$$V_{CM\_cont} = V_{CM\_in} - V_{GS1} - V_{DS,SAT\_5} + V_{GS\_5}$$
$$V_{CM\_cont} = V_{CM\_in} - V_{GS1} - (V_{GS\_5} - V_{TN\_5}) + V_{GS\_5}$$
$$V_{CM\_cont} = V_{CM\_in} - V_{GS1} + V_{TN\_5} \quad (5)$$

This allowed the conclusion that $V_{GS1} - V_{TN\_5}$ is the minimum voltage (minimum headroom) that V_{CM_Cont} must stay under the V_{CM_in}. [1]

The issue behind finding the $V_{GS1} - V_{TN\_5}$ is that the exact value of V_{TN_5} is unknown due to the back-gate effect. The goal was to estimate the value by using (1) but neglecting channel length modulation (λ). Now re-arranging the simplified (1) to solve for V_{TN_5}, (6) is possible. V_{GS_5} can be known as $V_{cont} - V_{S5}$, approximately 2V. Using (6) with every other known value, V_{TN_5} = 1.03V. Now V_{GS1} is equivalent to V_{CM_in} - V_{S1}, where $V_{S1} = V_{S5} + V_{DS5}$. Figure 13 provides an approximation of V_{DS5} = 2V at V_{CM_in} = 5.2V, and Figure 14 tells that V_{S5} is relatively constant at 1.08V. Combining the pieces together, this placed V_{S1} at 3.08V and V_{GS1} at 2.12V, setting $V_{GS1} - V_{TN\_5}$ at 1.09V. Thus, V_{CM_Cont} must stay at least 1.09V under V_{CM_in}. Accounting for some headroom, the proper V_{CM_Cont} range was determined to be from 3.0V to 4.0V.

$$I_{DQ5} = \frac{1}{2} * \mu Cox_n * \left(\frac{W}{L}\right)_5 (V_{GS\_5} - V_{TN\_5})^2$$

$$V_{TN\_5} = V_{GS\_5} - \sqrt{\frac{2*I_{DQ5}}{\mu Cox_n*\left(\frac{W}{L}\right)_5}} \quad (6)$$

IX. AC Response

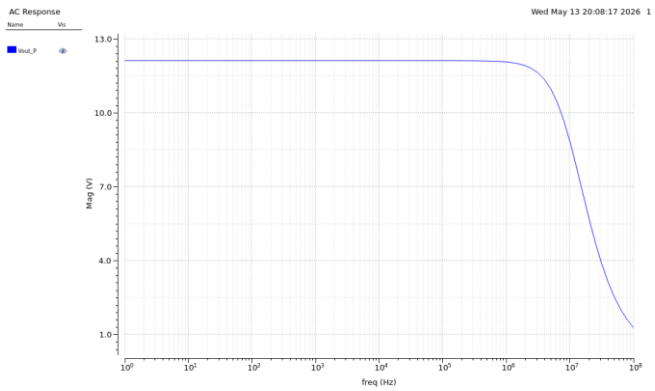

Fig. 15. Logarithmic plot of AC Gain in Volts

A. Gain and Phase

AC gain and phase were simulated in differential mode, that is, using an AC source with DC offset voltage of 5.2V and an AC amplitude of 1V at both inputs, with one input having an initial phase of 180 degrees to ensure differential operation. For full differential operation, the V_{cont} settings were changed to a single-ended input (V_{cont1}= 3.0V, V_{cont2} = 0.0V). This mode would steer all available current to one side, allowing for maximum gain at output. The target gain was calculated to be around 25. The AC amplitude of 1V allowed easy calculation for the AC gain, as the gain $Av = V_{out}/V_{in}$, if AC V_{in} = 1V, then Av is equivalent to the V_{out} itself. Figure 15 shows that the magnitude of the V_{out_p} itself was a little above 12V, which indicated that if the output were the differential signal between V_{out_p} and V_{out_n} Then the overall gain would double to ±24. This value reaches fairly close to the original target gain of ±25.

For the output to be a differential signal, as mentioned above, the amplifier must operate fully differentially. This was verified through plotting the AC gain magnitude and phase in dB and degrees, respectively. As seen in Figure 16, the gain magnitude is relatively consistent, while the output phases are 180 degrees apart.

B. Swing

Because the input is a sinusoidal differential signal, the output is also a sinusoidal differential signal; the output swings up and down from its Q-point. The maximum swing of the output is clamped by either the V_{outMAX} or the V_{outMIN}, whichever is touched first. Once the max swing is reached, the sinusoid-like output will experience distortion. This was observed after setting the V_{in_P} and V_{in_N} with a sinusoidal source of DC voltage of 5.2V and 20mV amplitude, 180-degree phase difference, and V_{cont} of 3V. The intent here was to increase the amplitude by 10mV steps until the V_{out} wave no longer inherited sinusoid characteristics. Around an amplitude of 40mV, the clipping behavior of V_{outMAX} was observed.

Figure 17 shows the transient analysis with all voltage sources operating at 1000 Hz and a 40 mV amplitude, for both cases when V_{cont1} is dominating the current and when $V_{cont2}$is dominating the current. As the gain is flipped, it was possible to confirm the proper functionality of the current steering by control FETs M5 and M6. The V_{outMAX} clipping behavior was observed as the magnitude of V_{outMIN} starts to

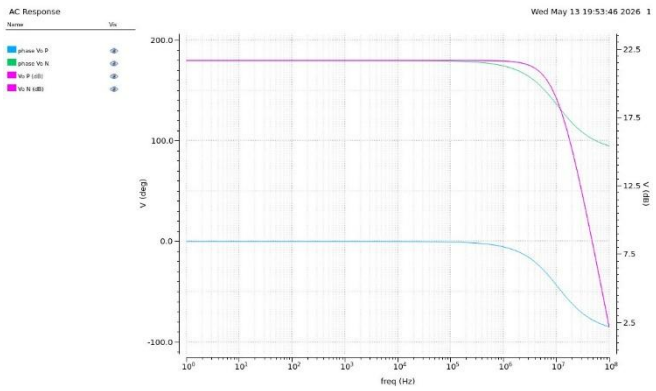

Fig. 16. Logarithmic plot of AC Gain in dB and phase

exceed the V_{outMAX}, placing the swing specification around ± 0.5V. This plot also verifies the differential operation of the amplifier, as the sinusoid waves of both V_{out_P} and V_{out_N} are out of phase from each other by 180 degrees.

X. Layout Process

This Gilbert Cell used FETs with fairly large W/L ratios. To approach the design, these large FETs were composed of multiple smaller-width (finger width) FETs connected in parallel. The diffused regions for drains or sources were shared as needed by the connection. In addition, all FETs experience different process gradients across the layout, leading to small variations among the devices. As an approach, the interdigitation process was utilized to minimize area and to average out characteristic differences due to process variations. When deciding on the finger width and the corresponding number of parallel connections, this interdigitation process is accounted for because the viability and quality of interdigitation can vary with the number of FETs and whether the total is odd or even.

There were 2 active loads (A and B), each with a width of 96 µm. This was implemented using a single 192 µm device composed of sixteen 12 µm finger-width devices connected in parallel, with drain terminals routed to different connections. A similar implementation was performed for the signal devices (M1–M4). Because there wasn't a point where all 4 devices shared both source and drain terminals, M1 and M2 formed a 40 µm device composed of four 10 µm finger-width devices, and the same held for M3 and M4. The control FETs (M5 & M6) used the same implementation as the active loads because their source terminals were shared. Together, they formed a 48 µm device composed of eight 6 µm finger-width devices.

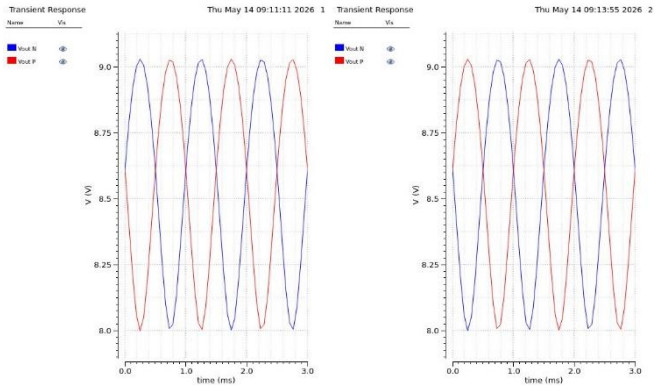

Fig. 17. Swing plot for Vcont1 = 3V (right), Vcont2 = 3V (left)

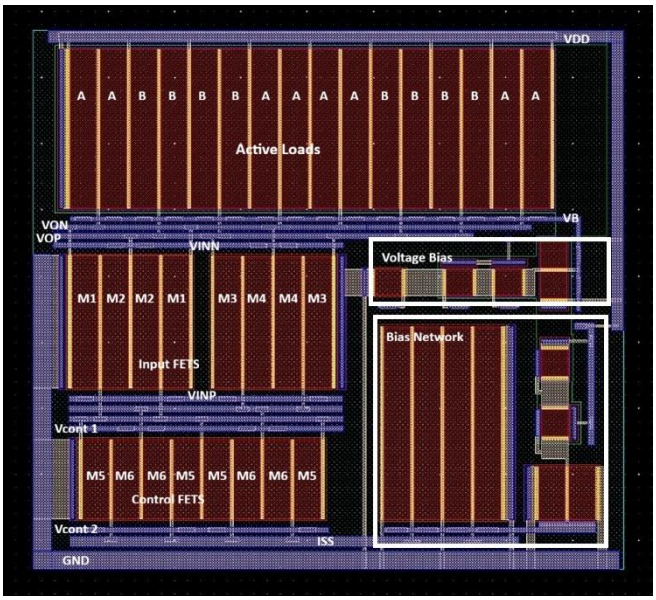

Fig. 18. Final Extracted Layout

XI. Layout Extraction and Evaluation

Figure 18 shows the final extracted layout of the devices in the circuit. Because back-gate effects were included, all p-FETs, including the bias network and V_B network, shared the same n-substrate-well. A and B are active load p-FETs. The extraction process also accounted for parasitic capacitances, which emerged as an issue when it caused an increase in the V_B of the voltage bias network to 8.5V. 0.2V difference might not look significant, but considering the square law relationship with V_{SG} from (1), the W/L requires a significant increase. But since W/L was consistent while parasitics caused a decrease in V_{SG}, I_{DQ} of the active load was no longer outputting the expected 365 µA; instead, it was outputting around 110 µA.

The layout was re-evaluated once by offsetting the V_B by near -0.2V to compensate for the 0.2V increase coming from the unwanted parasitic capacitance. To do so, using (1) again, the width of the top p-FET was decreased from 9 µm to 4 µm (W/L = 2), setting V_B = 8.07V. The final layout from Figure 18 is also the re-evaluation. The re-evaluated layout was simulated again, and Figures 19 and 20 show the VDS analysis and the AC response, respectively. The results showed that its behavior mostly matched the original simulation results from early parts of this paper.

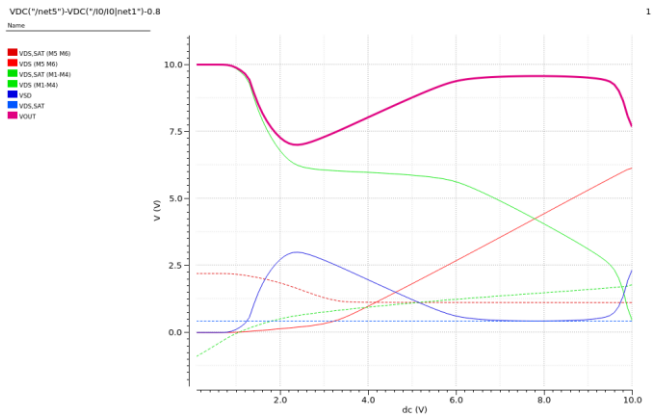

Fig. 19. VDS Analysis of the Extracted Layout.

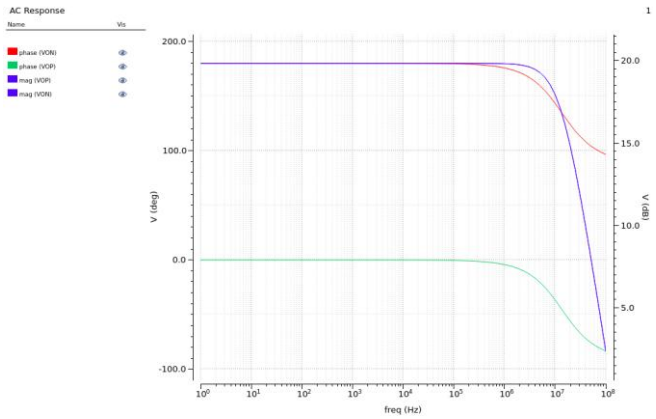

Fig. 20. AC Gain in dB and Phase for Extracted Layout.

Due to a slight variation in V_B, the Q-point for V_{out} at V_{CM_in} of 5.2V was slightly increased to 8.9V. To bring this back down close to the desired value of 8.6V, V_{CM_in} was adjusted to 4.8V. Simulation results in Figures 20 and 21 were all done under V_{CM_in} of 4.8V; the circuit produces a gain and swing slightly reduced from the original, and also inherits a slightly less flexible range of V_{CM_cont}, and this was most likely due to other parasitics that were not compensated during re-evaluation.

XII. Results

Figures 20 and 21 indicate the behavior of the final extracted layout of the Gilbert Cell, which exhibited an 8.56V Q-point, an AC gain magnitude range from -20 to +20 with differential output, and a max swing of ±0.48V. Figure 22 shows the differential signal of the output swing ($V_{out\_P} - V_{out_N}$), with various combinations of V_{cont}. When both V_{cont} are equal, the differential output is 0. It confirms proper differential operation of the outputs and the variable-gain capability as flips its polarity from changing V_{cont}. Table 3 shows the summarized comparison between the simulation results for the original circuit and the extracted layout.

XIII. Conclusion

The behavior of the final extracted layout, although it required minor adjustments to external voltages, generally matched the simulation. Even with slight gain and swing compensation, the primary goals of passing the design rule and layout-vs.-schematic checks, successfully extracting the layout, and re-evaluating the layout for proper functionality were achieved. More importantly, the insights from small aspects of device physics, such as short-channel effects, channel length modulation, and back-gate effects, were reinforced throughout the project as they were accounted for in the initial calculations. In addition, a variety of trade-offs were observed during the design process, such as the fact that decreasing a transistor parameter would almost always require increasing another. Overall, the logic and functionality of a Gilbert Cell were well understood.

TABLE III.

	VB (V)	V_{cont} Range (V)	Q-point (V)	Gain(V)	Swing (V)
Original	**8.3**	**3.0 – 4.0**	**8.6**	**±24**	**±0.5**
Layout	**8.27**	**3.0 – 3.7**	**8.56**	**±20**	**±0.48**

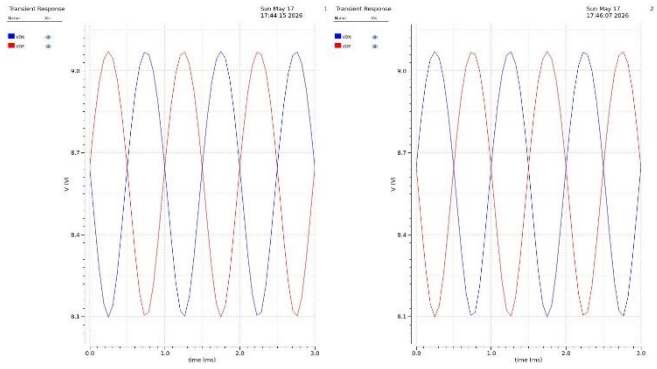

Fig. 21. Output Swing of Extracted Layout, Vcont1 = 3V, Vcont2 = 3V

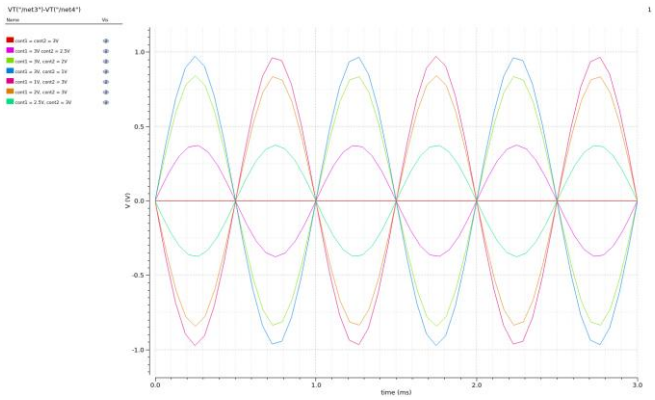

Fig. 22. Varying Differential Output Swing plot for Extracted Layout,

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